# ● PRINTER RUSH ●

**(PTO ASSISTANCE)**

IFW

**Application :** 09/841505 **Examiner :** DIMYAN **GAU :** 2825

**From:** QF **Location:** (IDC) FMF FDC **Date:** 8-29-05

Tracking #: CIC2408 Week Date: 6-6-05

| DOC CODE | DOC DATE | MISCELLANEOUS |
|---|---|---|
| ☐ 1449 | | ☐ Continuing Data |
| ☐ IDS | | ☐ Foreign Priority |
| ☐ CLM | | ☐ Document Legibility |
| ☐ IIFW | | ☐ Fees |
| ☐ SRFW | | ☐ Other |
| ☒ DRW | 4-24-01 | |
| ☐ OATH | | |
| ☐ 312 | | |
| ☐ SPEC | | |

[RUSH] **MESSAGE:** ATTN: Chief DRAFTSPERSON

Requesting new drawing sheets for all FIGURES- line thru drawings

THANK YOU

[XRUSH] **RESPONSE:** Drawings corrected

**INITIALS:** CBR

NOTE: This form will be included as part of the official USPTO record, with the Response document coded as XRUSH.

REV 10/04

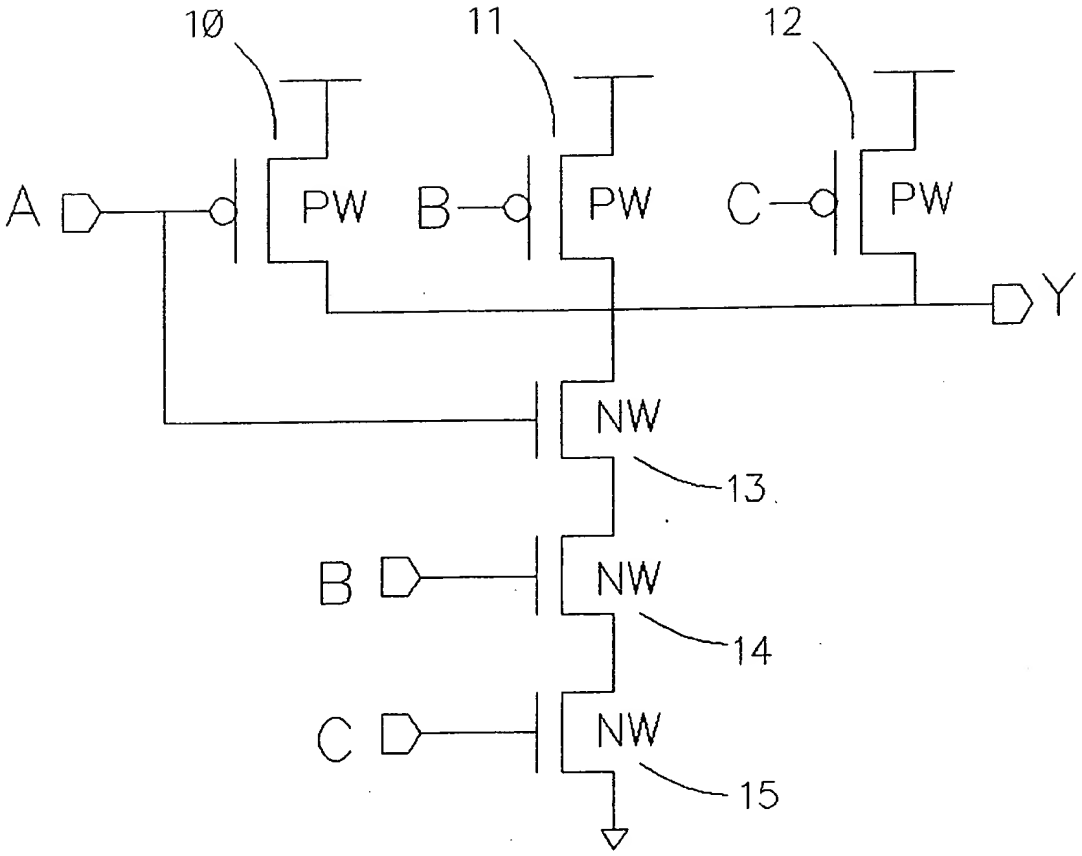


Fig 1. Non-tapered 3-input CMOS NAND gate

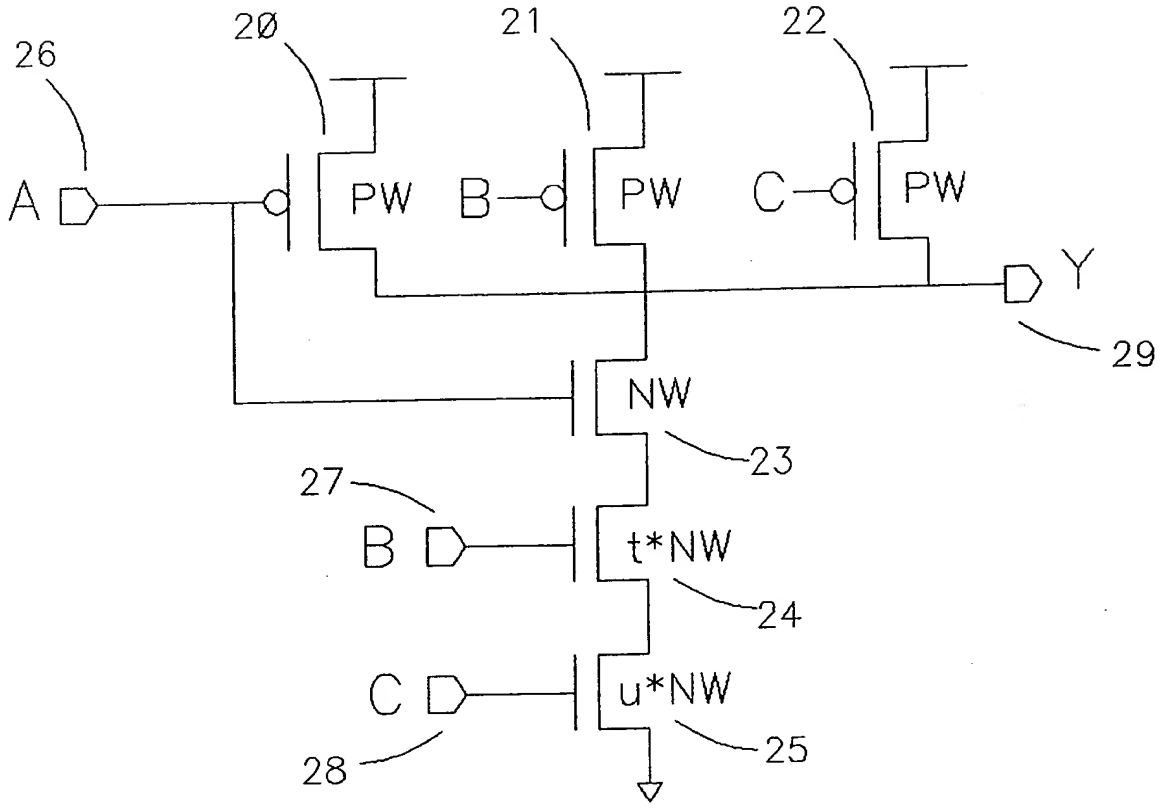


Fig 2. Tapered 3-input CMOS NAND gate

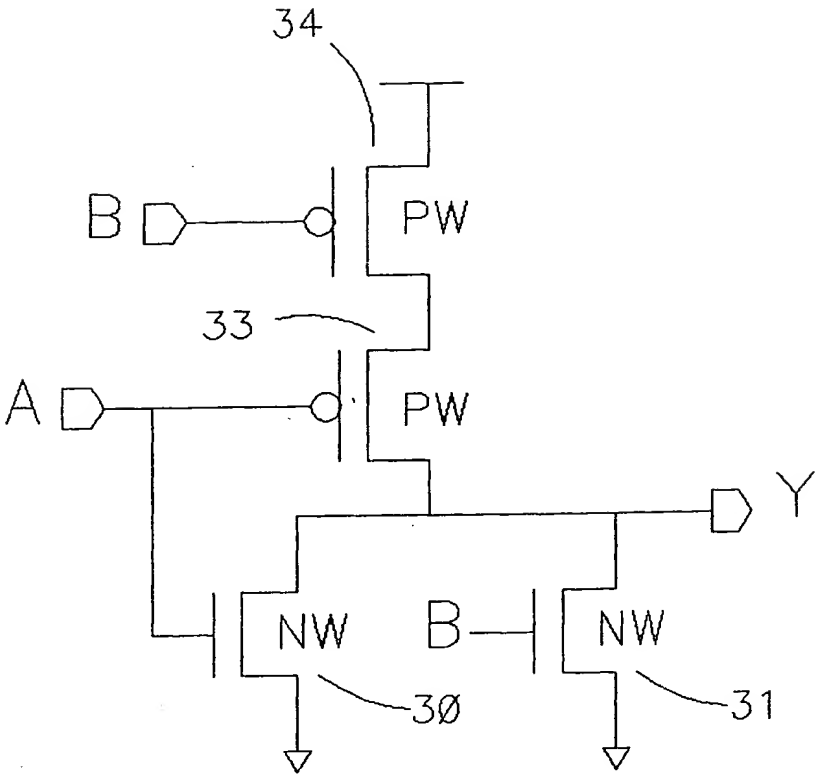


Fig 3. Non-tapered 2-input CMOS NOR gate

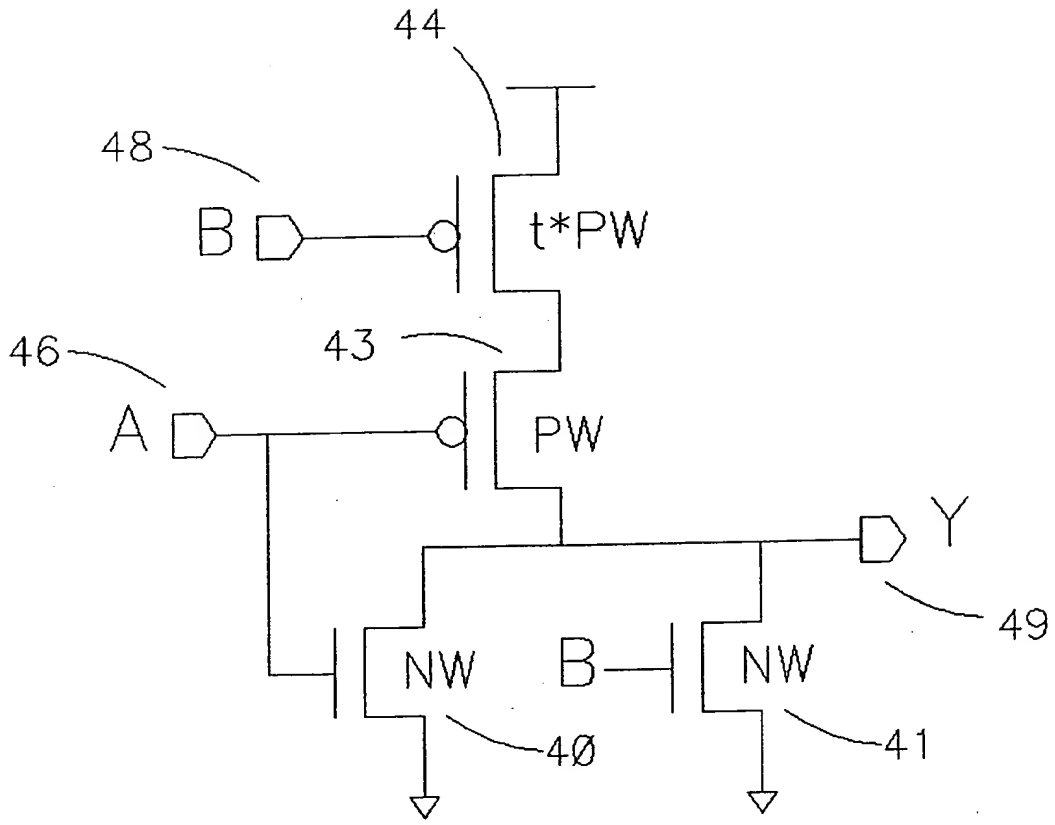


Fig 4. Tapered 2-input CMOS NOR gate

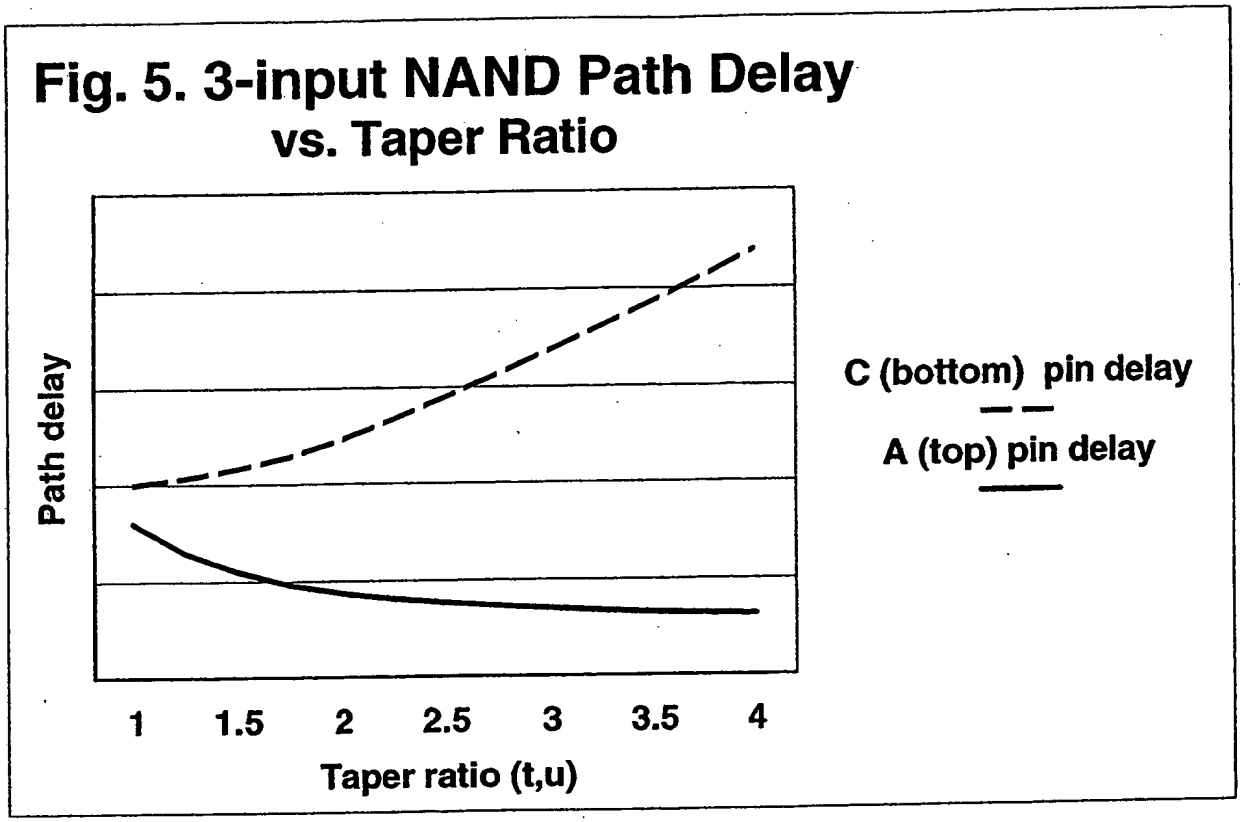
Fig. 5. 3-input NAND Path Delay
vs. Taper Ratio
Path delay
1
1.5
2
2.5
3
3.5
4
Taper ratio (t,u)
C (bottom) pin delay
A (top) pin delay

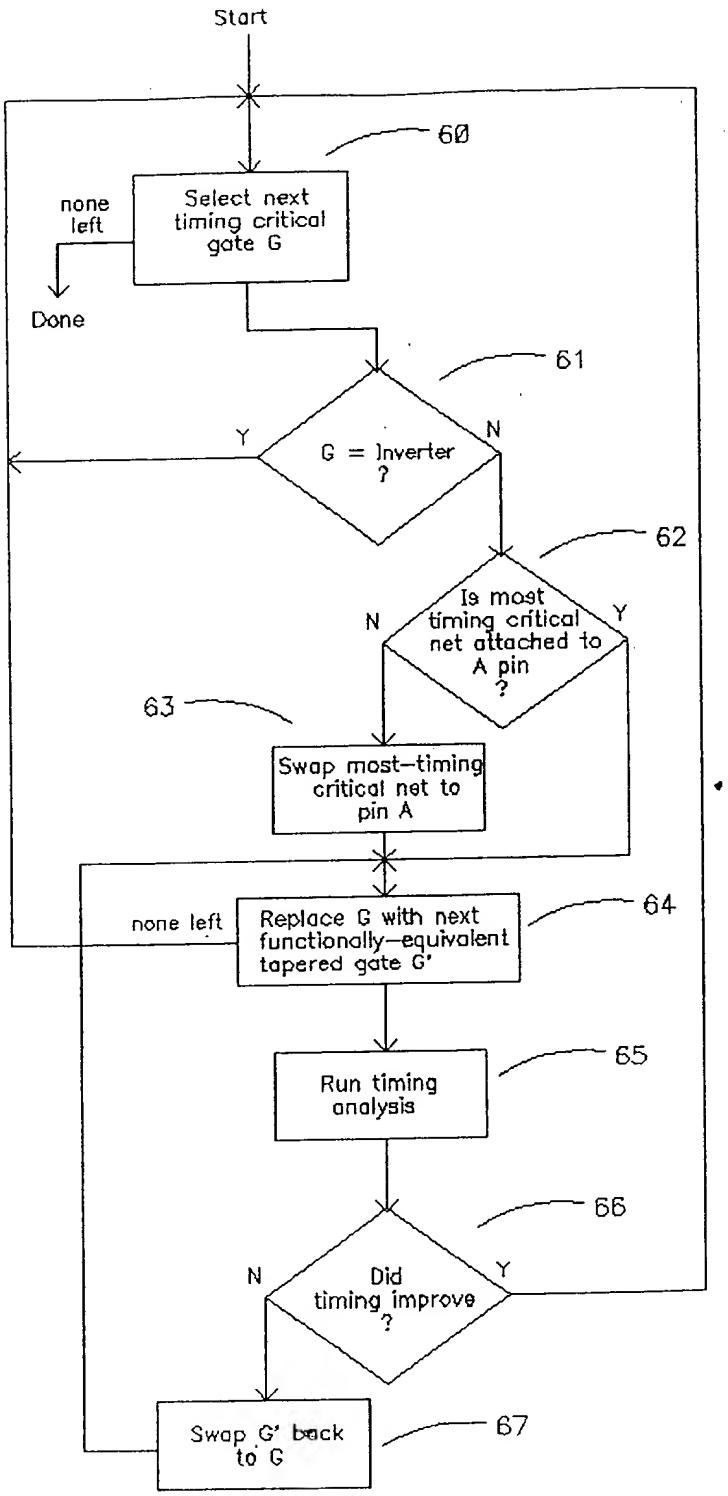


Fig 6. Synthesis tapered algorithm